Quad-Channel Isolators with Integrated DC-to-DC Converter

ADuM5401/ADuM5402/ADuM5403/ADuM5404

FEATURES

*iso*Power integrated, isolated dc-to-dc converter
Regulated 3.3 V or 5.0 V output
Up to 500 mW output power
Quad dc-to-25 Mbps (NRZ) signal isolation channels
Schmitt trigger inputs
16-lead SOIC package with >8.0 mm creepage
High temperature operation: 105°C
High common-mode transient immunity: >25 kV/μs
Safety and regulatory approvals
- UL recognition
  - 2500 V rms for 1 minute per UL1577
- CSA Component Acceptance Notice #5A (pending)
- VDE certificate of conformity (pending)
  - DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
  - V_{IORM} = 560 V peak

APPLICATIONS

RS-232/RS-422/RS-485 transceivers
Industrial field bus isolation
Power supply startup bias and gate drives
Isolated sensor interfaces
Industrial PLCs

GENERAL DESCRIPTION

The ADuM5401/ADuM5402/ADuM5403/ADuM5404[1] devices are quad-channel digital isolators with *iso*Power®, an integrated, isolated dc-to-dc converter. Based on the Analog Devices, Inc., *i*Coupler® technology, the dc-to-dc converter provides up to 500 mW of regulated, isolated power at either 5.0 V from a 5.0 V input supply or 3.3 V from a 3.3 V supply. This eliminates the need for a separate, isolated dc-to-dc converter in low power, isolated designs. The *i*Coupler chip scale transformer technology is used to isolate both the logic signals and the magnetic components of the dc-to-dc converter. The result is a small form factor, total isolation solution.

The ADuM5401/ADuM5402/ADuM5403/ADuM5404 isolators provide four independent isolation channels in a variety of channel configurations and data rates (see the Ordering Guide for more information).

*iso*Power uses high frequency switching elements to transfer power through its transformer. Special care must be taken during printed circuit board (PCB) layout to meet emissions standards. Refer to Application Note AN-0971 for details on board layout considerations.

FUNCTIONAL BLOCK DIAGRAMS

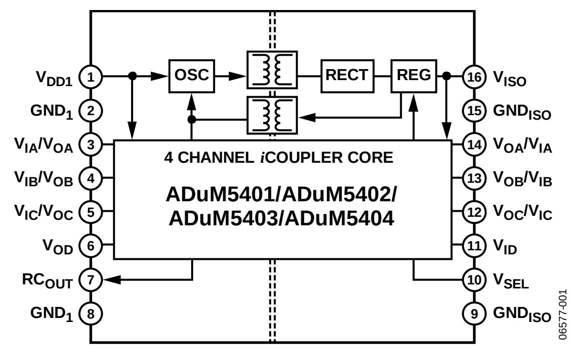


Figure 1. ADuM5401/ADuM5402/ADuM5403/ADuM5404

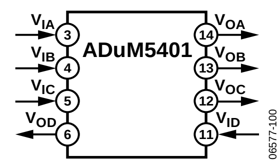


Figure 2. ADuM5401

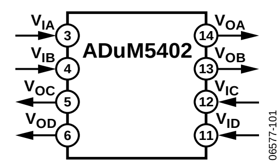


Figure 3. ADuM5402

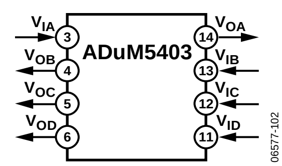


Figure 4. ADuM5403

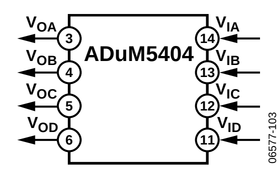


Figure 5. ADuM5404

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents are pending.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

11/08—Rev. 0 to Rev. A

Changes to Figure 1 and General Description Section ... 1
Changes to Table 1 ... 3
Changes to Table 2 ... 5
Changes to Table 4 ... 7
Changes to Table 6 and Table 7 ... 8
Changes to Table 8 and Table 9 ... 9
Changes to Figure 7 and Table 10 ... 10
Changes to Figure 8 and Table 11 ... 11
Changes to Figure 9 and Table 12 ... 12
Changes to Figure 10 and Table 13 ... 13
Moved Truth Table Section ... 13
Changes to Applications Information Section and PCB Layout Section ... 17
Changes to DC Correctness and Magnetic Field Immunity Section ... 18
Changes to Power Considerations Section ... 20
Added Increasing Available Power Section, Table 15, and Table 16 ... 20

5/08—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/5 V SECONDARY ISOLATED SUPPLY

4.5 V ≤ V_{DD1} ≤ 5.5 V, V_{SEL} = V_{ISO}; each voltage is relative to its respective ground. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = 5.0 V, V_{SEL} = V_{ISO}.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER POWER SUPPLY						
Setpoint	V_{ISO}	4.7	5.0	5.4	V	I_{ISO} = 0 mA
Line Regulation	$V_{ISO(LINE)}$		1		mV/V	I_{ISO} = 50 mA, V_{DD1} = 4.5 V to 5.5 V
Load Regulation	$V_{ISO(LOAD)}$		1	5	%	I_{ISO} = 10 mA to 90 mA
Output Ripple	$V_{ISO(RIP)}$		75		mV p-p	20 MHz bandwidth, C_{BO} = 0.1 µF || 10 µF, I_{ISO} = 90 mA
Output Noise	$V_{ISO(N)}$		200		mV p-p	C_{BO} = 0.1 µF || 10 µF, I_{ISO} = 90 mA
Switching Frequency	f_{OSC}		180		MHz	
Pulse-Width Modulation Frequency	f_{PWM}		625		kHz	
DC to 2 Mbps Data Rate[1]						
Maximum Output Supply Current[2]	$I_{ISO(MAX)}$	100			mA	V_{ISO} > 4.5 V, dc to 1 MHz logic signal frequency
Efficiency at Maximum Output Supply Current[3]			34		%	I_{ISO} = 100 mA, dc to 1 MHz logic signal frequency
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1(Q)}$		19	30	mA	I_{ISO} = 0 mA, dc to 1 MHz logic signal frequency
I_{DD1} Supply Current, Full V_{ISO} Load	$I_{DD1(MAX)}$		290		mA	C_L = 0 pF, dc to 1 MHz logic signal frequency, V_{DD} = 4.5 V, I_{ISO} = 100 mA
25 Mbps Data Rate (CRWZ Grade Only)						
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1(D)}$					
ADuM5401			68		mA	I_{ISO} = 0 mA, C_L = 15 pF, 12.5 MHz logic signal frequency
ADuM5402			71		mA	I_{ISO} = 0 mA, C_L = 15 pF, 12.5 MHz logic signal frequency
ADuM5403			75		mA	I_{ISO} = 0 mA, C_L = 15 pF, 12.5 MHz logic signal frequency
ADuM5404			78		mA	I_{ISO} = 0 mA, C_L = 15 pF, 12.5 MHz logic signal frequency
Available V_{ISO} Supply Current[4]	$I_{ISO(LOAD)}$					
ADuM5401			87		mA	C_L = 15 pF, 12.5 MHz logic signal frequency
ADuM5402			85		mA	C_L = 15 pF, 12.5 MHz logic signal frequency
ADuM5403			83		mA	C_L = 15 pF, 12.5 MHz logic signal frequency
ADuM5404			81		mA	C_L = 15 pF, 12.5 MHz logic signal frequency
Undervoltage Lockout, V_{DD1}, V_{DDL}, and V_{ISO} Supply						
Positive Going Threshold	V_{UV+}		2.7		V	
Negative Going Threshold	V_{UV-}		2.4		V	
Hysteresis	V_{UVH}		0.3		V	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
*i*COUPLER DATA CHANNELS						
I/O Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}	−20	+0.01	+20	µA	
Logic High Input Threshold	V_{IH}	$0.7 \times V_{ISO}$, $0.7 \times V_{IDD1}$			V	
Logic Low Input Threshold	V_{IL}			$0.3 \times V_{ISO}$, $0.3 \times V_{IDD1}$	V	
Logic High Output Voltages	RC_{OUT}, V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	$V_{DD1} - 0.3$, $V_{ISO} - 0.3$	5.0		V	$I_{Ox} = -20$ µA, $V_{Ix} = V_{IxH}$
		$V_{DD1} - 0.5$, $V_{ISO} - 0.5$	4.8		V	$I_{Ox} = -4$ mA, $V_{Ix} = V_{IxH}$
Logic Low Output Voltages	RC_{OUT}, V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	$I_{Ox} = 20$ µA, $V_{Ix} = V_{IxL}$
			0.0	0.4	V	$I_{Ox} = 4$ mA, $V_{Ix} = V_{IxL}$
AC SPECIFICATIONS						
ARWZ Grade Only						
Minimum Pulse Width	PW			1000	ns	$C_L = 15$ pF, CMOS signal levels
Maximum Data Rate		1			Mbps	$C_L = 15$ pF, CMOS signal levels
Propagation Delay	t_{PHL}, t_{PLH}		55	100	ns	$C_L = 15$ pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			40	ns	$C_L = 15$ pF, CMOS signal levels
Propagation Delay Skew	t_{PSK}			50	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching	t_{PSKCD}/t_{PSKOD}			50	ns	$C_L = 15$ pF, CMOS signal levels
CRWZ Grade Only						
Minimum Pulse Width	PW			40	ns	$C_L = 15$ pF, CMOS signal levels
Maximum Data Rate		25			Mbps	$C_L = 15$ pF, CMOS signal levels
Propagation Delay	t_{PHL}, t_{PLH}		45	60	ns	$C_L = 15$ pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			6	ns	$C_L = 15$ pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	$C_L = 15$ pF, CMOS signal levels
Propagation Delay Skew	t_{PSK}			15	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels	t_{PSKCD}			6	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching, Opposing Directional Channels	t_{PSKOD}			15	ns	$C_L = 15$ pF, CMOS signal levels
For All Models						
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	$C_L = 15$ pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output	$\|CM_H\|$	25	35		kV/µs	$V_{Ix} = V_{DD}$ or V_{ISO}, $V_{CM} = 1000$ V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	25	35		kV/µs	$V_{Ix} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V
Refresh Rate	f_r		1.0		Mbps	

[1] The contributions of supply current values for all four channels are combined at identical data rates.
[2] The V_{ISO} supply current is available for external use when all data rates are below 2 Mbps. At data rates above 2 Mbps, the data I/O channels draw additional current proportional to the data rate. Additional supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. The dynamic I/O channel load must be treated as an external load and included in the V_{ISO} power budget.
[3] The power demands of the quiescent operation of the data channels cannot be separated from the power supply section. Efficiency includes the quiescent power consumed by the I/O channels as part of the internal power consumption.
[4] This current is available for driving external loads at the V_{ISO} pin. All channels are simultaneously driven at a maximum data rate of 25 Mbps with full capacitive load representing the maximum dynamic load conditions. Refer to the Power Consumption section for calculation of available current at less than the maximum data rate.

ELECTRICAL CHARACTERISTICS—3.3 V PRIMARY INPUT SUPPLY/3.3 V SECONDARY ISOLATED SUPPLY

3.0 V ≤ V_{DD1} ≤ 3.6 V, V_{SEL} = GND_{ISO}; each voltage is relative to its respective ground. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = 3.3 V, V_{ISO} = 3.3 V, V_{SEL} = GND_{ISO}.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER POWER SUPPLY						
Setpoint	V_{ISO}	3.0	3.3	3.6	V	I_{ISO} = 0 mA
Line Regulation	$V_{ISO(LINE)}$		1		mV/V	I_{ISO} = 30 mA, V_{DD1} = 3.0 V to 3.6 V
Load Regulation	$V_{ISO(LOAD)}$		1	5	%	I_{ISO} = 6 mA to 54 mA
Output Ripple	$V_{ISO(RIP)}$		50		mV p-p	20 MHz bandwidth, C_{BO} = 0.1 µF || 10 µF, I_{ISO} = 54 mA
Output Noise	$V_{ISO(N)}$		130		mV p-p	C_{BO} = 0.1 µF || 10 µF, I_{ISO} = 54 mA
Switching Frequency	f_{OSC}		180		MHz	
Pulse-Width Modulation Frequency	f_{PWM}		625		kHz	
DC to 2 Mbps Data Rate[1]						
Maximum Output Supply Current[2]	$I_{ISO(MAX)}$	60			mA	V_{ISO} > 3.0 V, dc to 1 MHz logic signal frequency,
Efficiency at Maximum Output Supply Current[3]			36		%	I_{ISO} = 60 mA, dc to 1 MHz logic signal frequency
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1(Q)}$		14	20	mA	I_{ISO} = 0 mA, dc to 1 MHz logic signal frequency
I_{DD1} Supply Current, Full V_{ISO} Load	$I_{DD1(MAX)}$		175		mA	C_L = 0 pF, dc to 1 MHz logic signal frequency, V_{DD} = 3.0 V, I_{ISO} = 60 mA
Power at 25 Mbps Data Rate						
25 Mbps Data Rate (CRWZ Grade Only)						
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1(D)}$					
ADuM5401			44		mA	I_{ISO} = 0 mA, C_L = 15 pF, 12.5 MHz logic signal frequency
ADuM5402			46		mA	I_{ISO} = 0 mA, C_L = 15 pF, 12.5 MHz logic signal frequency
ADuM5403			47		mA	I_{ISO} = 0 mA, C_L = 15 pF, 12.5 MHz logic signal frequency
ADuM5404			51		mA	I_{ISO} = 0 mA, C_L = 15 pF, 12.5 MHz logic signal frequency
Available V_{ISO} Supply Current[4]						
ADuM5401	$I_{ISO(LOAD)}$		42		mA	C_L = 15 pF, 12.5 MHz logic signal frequency
ADuM5402	$I_{ISO(LOAD)}$		41		mA	C_L = 15 pF, 12.5 MHz logic signal frequency
ADuM5403	$I_{ISO(LOAD)}$		39		mA	C_L = 15 pF, 12.5 MHz logic signal frequency
ADuM5404	$I_{ISO(LOAD)}$		38		mA	C_L = 15 pF, 12.5 MHz logic signal frequency
Undervoltage Lockout, V_{DD1},V_{DDL}, and V_{ISO} Supply						
Positive Going Threshold	V_{UV+}		2.7		V	
Negative Going Threshold	V_{UV-}		2.4		V	
Hysteresis	V_{UVH}		0.3		V	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
*i*COUPLER DATA CHANNELS						
I/O Input Currents	I_{IA}, I_{IB}, I_{IC}, $I_{ID,}$	−10	+0.01	+10	µA	
Logic High Input Threshold	V_{IH}	0.7 × V_{ISO}, 0.7 × V_{IDD1}			V	
Logic Low Input Threshold	V_{IL}			0.3 × V_{ISO}, 0.3 × V_{IDD1}	V	
Logic High Output Voltages	RC_{OUT}, V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	V_{DD1} − 0.3, V_{ISO} − 0.3	3.3		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DD1} − 0.5, V_{1SO} − 0.5	3.1		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	RC_{OUT}, V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.0	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
AC SPECIFICATIONS						
ARWZ Grade Only						
Minimum Pulse Width	PW			1000	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay	t_{PHL}, t_{PLH}		60	100	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			40	ns	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew	t_{PSK}			50	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching	t_{PSKCD}/t_{PSKOD}			50	ns	C_L = 15 pF, CMOS signal levels
CRWZ Grade Only						
Minimum Pulse Width	PW			40	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate		25			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay	t_{PHL}, t_{PLH}		45	60	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			6	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew	t_{PSK}			45	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels	t_{PSKCD}			6	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing Directional Channels	t_{PSKOD}			15	ns	C_L = 15 pF, CMOS signal levels
For All Models						
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output	$\|CM_H\|$	25	35		kV/µs	V_{Ix} = V_{DD} or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.0		Mbps	

[1] The contributions of supply current values for all four channels are combined at identical data rates.
[2] The V_{ISO} supply current is available for external use when all data rates are below 2 Mbps. At data rates above 2 Mbps, the data I/O channels draw additional current proportional to the data rate. Additional supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. The dynamic I/O channel load must be treated as an external load and included in the V_{ISO} power budget.
[3] The power demands of the quiescent operation of the data channels cannot be separated from the power supply section. Efficiency includes the quiescent power consumed by the I/O channels as part of the internal power consumption.
[4] This current is available for driving external loads at the V_{ISO} pin. All channels are simultaneously driven at a maximum data rate of 25 Mbps with full capacitive load representing the maximum dynamic load conditions. Refer to the Power Consumption section for calculation of available current at less than the maximum data rate.

PACKAGE CHARACTERISTICS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input to Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction-to-Ambient Thermal Resistance	$θ_{JA}$		45		°C/W	Thermocouple located at center of package underside, test conducted on 4-layer board with thin traces[3]

[1] The device is considered a 2-terminal device: Pin 1 to Pin 8 are shorted together, and Pin 9 to Pin 16 are shorted together.
[2] Input capacitance is from any input data pin to ground.
[3] See the Thermal Analysis section for thermal model definitions.

REGULATORY APPROVALS

Table 4.

UL	CSA (Pending)	VDE (Pending)
Recognized under the UL1577 component recognition program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]
Single protection, 2500 V rms isolation voltage	Reinforced insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (566 V peak) maximum working voltage	Reinforced insulation, 560 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL1577, each ADuM5401/ADuM5402/ADuM5403/ADuM5404 is proof tested by applying an insulation test voltage of ≥3000 V rms for 1 sec (current leakage detection limit = 10 µA).
[2] In accordance with DIN V VDE V 0884-10, each of the ADuM5401/ADuM5402/ADuM5403/ADuM5404 is proof tested by applying an insulation test voltage of ≥1050 V peak for 1 sec (partial discharge detection limit = 5 pC). The asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 5.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	>8.0	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	>8.0	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017	mm min	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303, Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marking on packages denotes DIN V VDE V 0884-10 approval.

Table 6.

Description	Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V peak
Input-to-Output Test Voltage, Method b1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, t_m = 1 sec, partial discharge < 5 pC	V_{PR}	1050	V peak
Input-to-Output Test Voltage, Method a		V_{PR}		
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC		896	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC		672	V peak
Highest Allowable Overvoltage	Transient overvoltage, t_{TR} = 10 sec	V_{TR}	4000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 6)			
Case Temperature		T_S	150	°C
Side 1 I_{DD1} Current		I_{S1}	555	mA
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

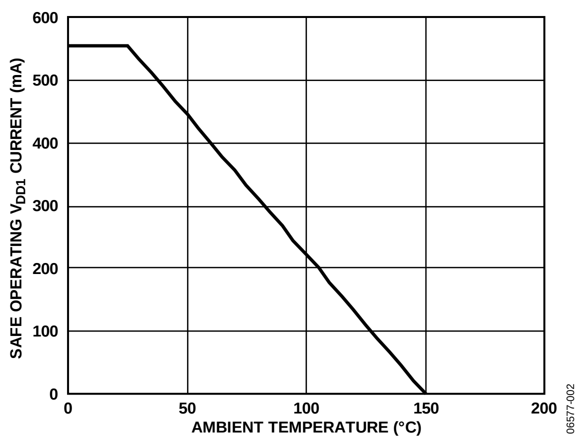


Figure 6. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN EN 60747-5-2

RECOMMENDED OPERATING CONDITIONS

Table 7.

Parameter	Symbol	Min	Max	Unit
Operating Temperature[1]	T_A	−40	+85	°C
Supply Voltages[2]				
V_{DD1} @ V_{SEL} = 0 V	V_{DD1}	3.0	3.6	V
V_{DD1} @ V_{SEL} = V_{ISO}	V_{DD1}	4.5	5.5	V
Minimum Load[3]	$I_{ISO(MIN)}$	10		mA

[1] Operation at 105°C requires reduction of the maximum load current, as specified in Table 8.
[2] All voltages are relative to their respective ground.
[3] If the external load is less than the specified value, the power supply PWM can generate excess switching noise, potentially causing data integrity issues.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
Storage Temperature (T_{ST})	−55°C to +150°C
Ambient Operating Temperature (T_A)	−40°C to +105°C
Supply Voltages (V_{DD}, V_{ISO})[1]	−0.5 V to +7.0 V
V_{ISO} Supply Current[2]	
T_A = −40°C to +85°C	100 mA
T_A = −40°C to +105°C	60 mA
Input Voltage (V_{IA}, V_{IB}, V_{IC}, V_{ID}, V_{SEL})[1, 3]	−0.5 V to V_{DDI} + 0.5 V
Output Voltage (RC_{OUT}, V_{OA}, V_{OB}, V_{OC}, V_{OD})[1, 3]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current Per Data Output Pin[4]	−10 mA to +10 mA
Common-Mode Transients[5]	−100 kV/µs to +100 kV/µs

[1] All voltages are relative to their respective ground.

[2] The V_{ISO} provides current for dc and dynamic loads on the V_{ISO} I/O channels. This current must be included when determining the total V_{ISO} supply current. For ambient temperatures between 85°C and 105°C, maximum allowed current is reduced.

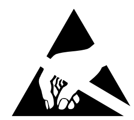
[3] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively. See the PCB Layout section.

[4] See Figure 6 for the maximum rated current values for various temperatures.

[5] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 9. Maximum Continuous Working Voltage Supporting 50-Year Minimum Lifetime[1]

Parameter	Maximum	Unit	Reference Standard
AC Voltage			
Reinforced Insulation	424	V peak	All certifications
Unipolar AC Voltage			
Basic Insulation	600	V peak	Working voltage per IEC 60950-1
Reinforced Insulation	560	V peak	Working voltage per VDE V 0884-10
DC Voltage			
Basic Insulation	600	V peak	Working voltage per IEC 60950-1
Reinforced Insulation	560	V peak	Working voltage per VDE V 0884-10

[1] Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more information.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

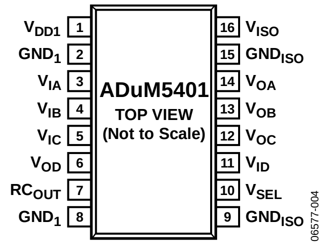


Figure 7. ADuM5401 Pin Configuration

Table 10. ADuM5401 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Primary Supply Voltage, 3.0 V to 5.5 V.
2, 8	GND_1	Ground 1. Ground reference for isolator primary. Pin 2 and Pin 8 are internally connected to each other. It is recommended that both pins be connected to a common ground.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{IC}	Logic Input C.
6	V_{OD}	Logic Output D.
7	RC_{OUT}	Regulation Control Output. This pin is connected to the RC_{IN} of a slave *iso*Power device to allow the ADuM5401 to control the regulation of the slave device.
9, 15	GND_{ISO}	Ground Reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected to each other. It is recommended that both pins be connected to a common ground.
10	V_{SEL}	Output Voltage Selection. When $V_{SEL} = V_{ISO}$, the V_{ISO} setpoint is 5.0 V. When $V_{SEL} = GND_{ISO}$, the V_{ISO} setpoint is 3.3 V.
11	V_{ID}	Logic Input D.
12	V_{OC}	Logic Output C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
16	V_{ISO}	Secondary Supply Voltage Output for Data Channels and External Loads.

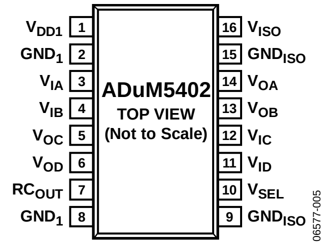


Figure 8. ADuM5402 Pin Configuration

Table 11. ADuM5402 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Primary Supply Voltage, 3.0 V to 5.5 V.
2, 8	GND_1	Ground 1. Ground reference for isolator primary. Pin 2 and Pin 8 are internally connected to each other. It is recommended that both pins be connected to a common ground.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{OC}	Logic Output C.
6	V_{OD}	Logic Output D.
7	RC_{OUT}	Regulation Control Output. This pin is connected to the RC_{IN} of a slave *iso*Power device to allow the ADuM5402 to control the regulation of the slave device.
9, 15	GND_{ISO}	Ground Reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected to each other. It is recommended that both pins be connected to a common ground.
10	V_{SEL}	Output Voltage Selection. When V_{SEL} = V_{ISO}, the V_{ISO} setpoint is 5.0 V. When V_{SEL} = GND_{ISO}, the V_{ISO} setpoint is 3.3 V.
11	V_{ID}	Logic Input D.
12	V_{IC}	Logic Input C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
16	V_{ISO}	Secondary Supply Voltage Output for Data Channels and External Loads.

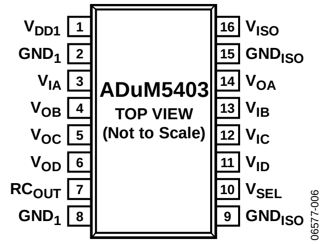


Figure 9. ADuM5403 Pin Configuration

Table 12. ADuM5403 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Primary Supply Voltage, 3.0 V to 5.5 V.
2, 8	GND_1	Ground 1. Ground reference for isolator primary. Pin 2 and Pin 8 are internally connected to each other. It is recommended that both pins be connected to a common ground.
3	V_{IA}	Logic Input A.
4	V_{OB}	Logic Output B.
5	V_{OC}	Logic Output C.
6	V_{OD}	Logic Output D.
7	RC_{OUT}	Regulation Control Output. This pin is connected to the RC_{IN} of a slave *iso*Power device to allow the ADuM5403 to control the regulation of the slave device.
9, 15	GND_{ISO}	Ground Reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected to each other. It is recommended that both pins be connected to a common ground.
10	V_{SEL}	Output Voltage Selection. When $V_{SEL} = V_{ISO}$, the V_{ISO} setpoint is 5.0 V. When $V_{SEL} = GND_{ISO}$, the V_{ISO} setpoint is 3.3 V.
11	V_{ID}	Logic Input D.
12	V_{IC}	Logic Input C.
13	V_{IB}	Logic Input B.
14	V_{OA}	Logic Output A.
16	V_{ISO}	Secondary Supply Voltage Output for Data Channels and External Loads.

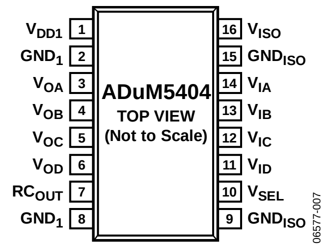


Figure 10. ADuM5404 Pin Configuration

Table 13. ADuM5404 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Primary Supply Voltage, 3.0 V to 5.5 V.
2, 8	GND_1	Ground 1. Ground reference for isolator primary. Pin 2 and Pin 8 are internally connected to each other. It is recommended that both pins be connected to a common ground.
3	V_{OA}	Logic Output A.
4	V_{OB}	Logic Output B.
5	V_{OC}	Logic Output C.
6	V_{OD}	Logic Output D.
7	RC_{OUT}	Regulation Control Output. This pin is connected to the RC_{IN} of a slave *iso*Power device to allow the ADuM5404 to control the regulation of the slave device.
9, 15	GND_{ISO}	Ground Reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected to each other. It is recommended that both pins be connected to a common ground.
10	V_{SEL}	Output Voltage Selection. When $V_{SEL} = V_{ISO}$, the V_{ISO} setpoint is 5.0 V. When $V_{SEL} = GND_{ISO}$, the V_{ISO} setpoint is 3.3 V.
11	V_{ID}	Logic Input D.
12	V_{IC}	Logic Input C.
13	V_{IB}	Logic Input B.
14	V_{IA}	Logic Input A.
16	V_{ISO}	Secondary Supply Voltage Output for Data Channels and External Loads.

TRUTH TABLE

Table 14. Truth Table (Positive Logic)

V_{Ix} Input[1]	V_{SEL} Input	V_{DD1} State	V_{DD1} Input (V)	V_{ISO} State	V_{ISO} Output (V)	V_{Ox} Output[1]	Notes
High	High	Powered	5.0	Powered	5.0	High	Normal operation, data is high
Low	High	Powered	5.0	Powered	5.0	Low	Normal operation, data is low
High	Low	Powered	3.3	Powered	3.3	High	Normal operation, data is high
Low	Low	Powered	3.3	Powered	3.3	Low	Normal operation, data is low
High	Low	Powered	5.0	Powered	3.3	High	Configuration not recommended
Low	Low	Powered	5.0	Powered	3.3	Low	Configuration not recommended
High	High	Powered	3.3	Powered	5.0	High	Configuration not recommended
Low	High	Powered	3.3	Powered	5.0	Low	Configuration not recommended

[1] V_{Ix} and V_{Ox} refer to the input and output signals of a given channel (A, B, C, or D).

TYPICAL PERFORMANCE CHARACTERISTICS

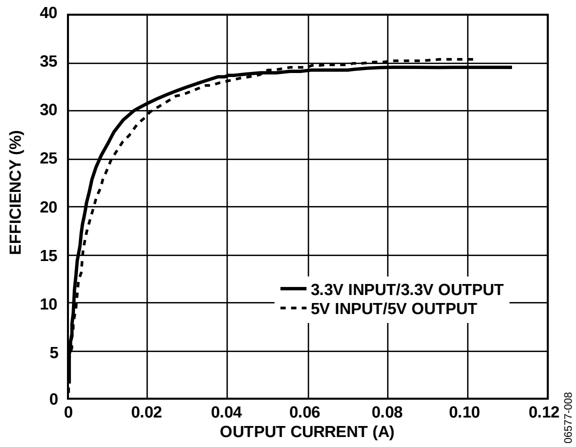


Figure 11. Typical Power Supply Efficiency at 5 V INPUT/5 V OUTPUT and 3.3 V INPUT/3.3 V OUTPUT

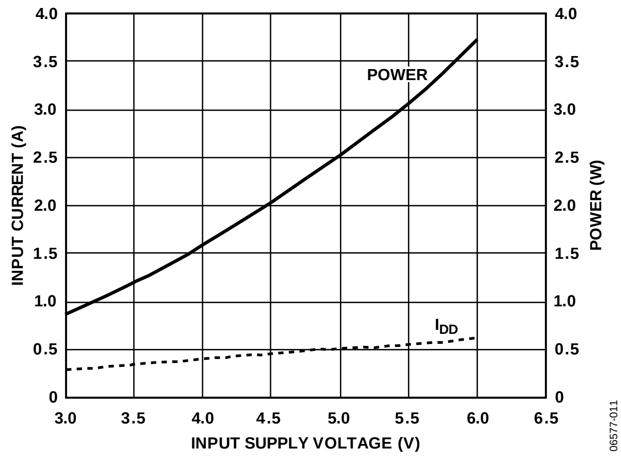


Figure 14. Typical Short-Circuit Input Current and Power vs. Input Supply Voltage, V_{ISO} shorted to GND_{ISO}

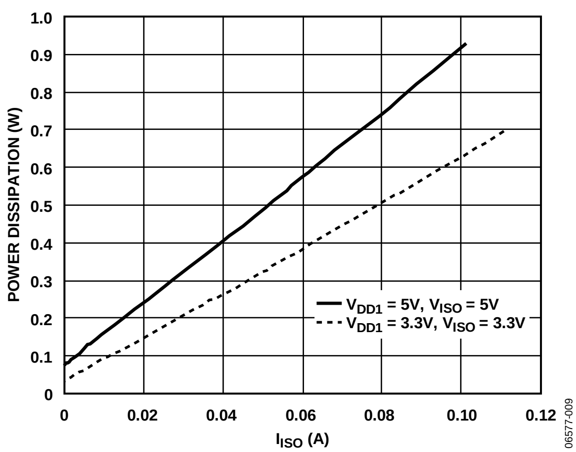


Figure 12. Typical Total Power Dissipation vs. I_{ISO} with Data Channels Idle

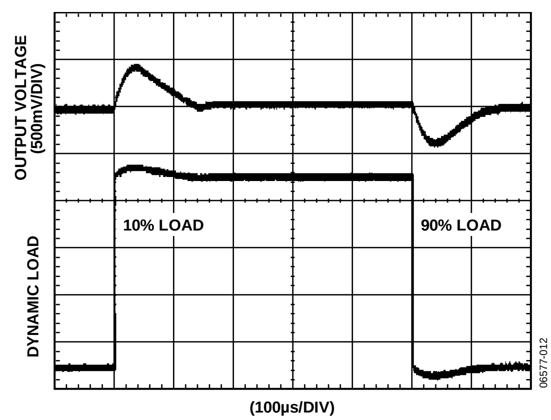


Figure 15. Typical V_{ISO} Transient Load Response, 5 V Output, 10% to 90% Load Step

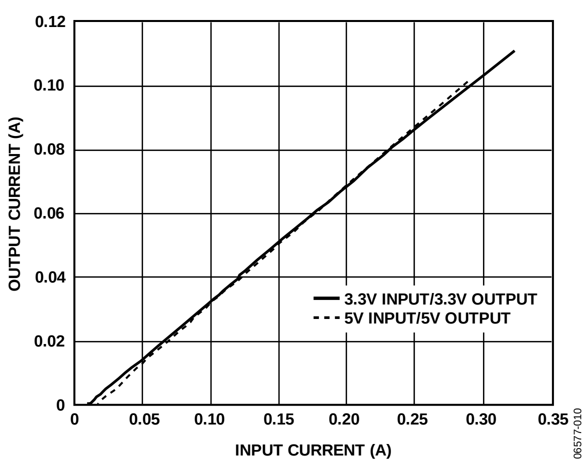


Figure 13. Typical Isolated Output Supply Current, I_{ISO}, as a Function of External Load, No Dynamic Current Draw at 5 V INPUT/5 V OUTPUT and 3.3 V INPUT/3.3 V OUTPUT

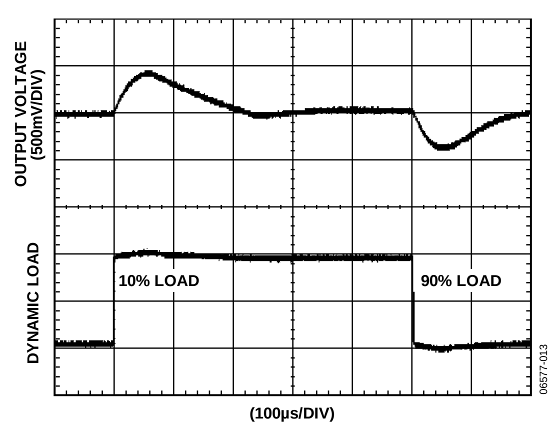


Figure 16. Typical Transient Load Response, 3 V Output, 10% to 90% Load Step

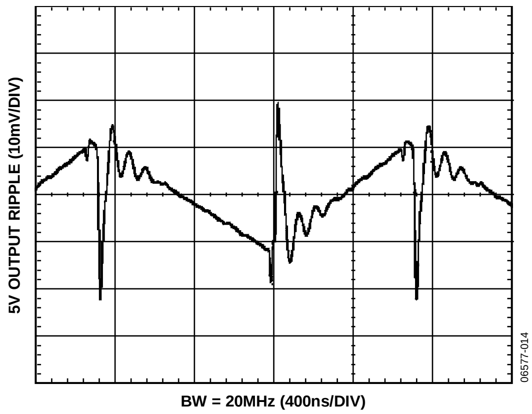


Figure 17. Typical V_{ISO} = 5 V Output Voltage Ripple at 90% Load

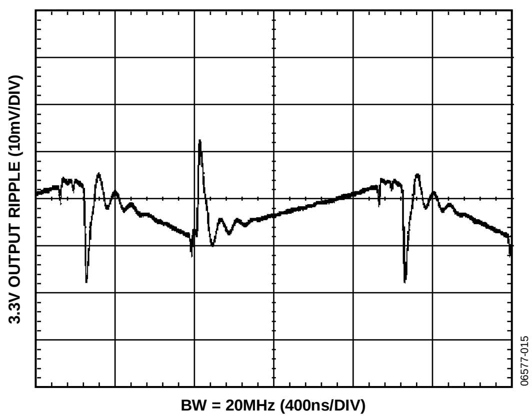


Figure 18. Typical V_{ISO} = 3.3 V Output Voltage Ripple at 90% Load

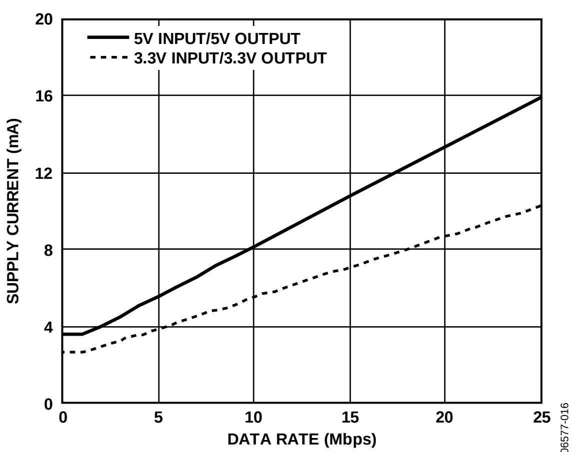


Figure 19. Typical I_{CH} Supply Current per Forward Data Channel (15 pF Output Load)

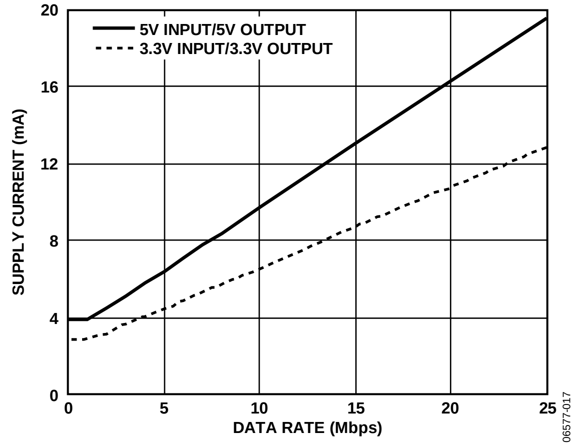


Figure 20. Typical I_{CH} Supply Current per Reverse Data Channel (15 pF Output Load)

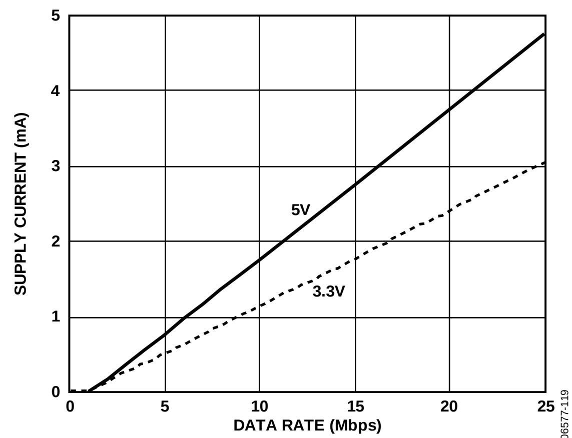


Figure 21. Typical $I_{ISO(D)}$ Dynamic Supply Current per Input

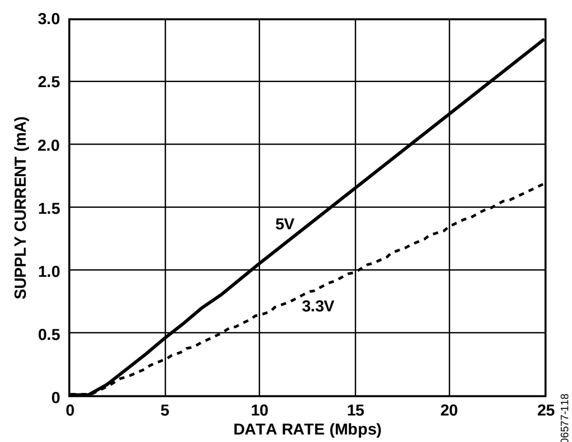


Figure 22. Typical $I_{ISO(D)}$ Dynamic Supply Current per Output (15 pF Output Load)

TERMINOLOGY

$I_{DD1(Q)}$

$I_{DD1(Q)}$ is the minimum operating current drawn at the V_{DD1} pin when there is no external load at V_{ISO} and the I/O pins are operating below 2 Mbps, requiring no additional dynamic supply current. $I_{DD1(Q)}$ reflects the minimum current operating condition.

$I_{DD1(D)}$

$I_{DD1(D)}$ is the typical input supply current with all channels simultaneously driven at maximum data rate of 25 Mbps with full capacitive load representing the maximum dynamic load conditions. Resistive loads on the outputs should be treated separately from the dynamic load.

$I_{DD1(MAX)}$

$I_{DD1(MAX)}$ is the input current under full dynamic and V_{ISO} load conditions.

t_{PHL} Propagation Delay

t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal.

t_{PLH} Propagation Delay

t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.

Propagation Delay Skew (t_{PSK})

t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Channel-to-Channel Matching

Channel-to-channel matching is the absolute value of the difference in propagation delays between the two channels when operated with identical loads.

Minimum Pulse Width

The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

Maximum Data Rate

The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

APPLICATIONS INFORMATION

The dc-to-dc converter section of the ADuM5401/ADuM5402/ADuM5403/ADuM5404 works on principles that are common to most modern power supplies. It is a secondary side controller architecture with isolated pulse-width modulation (PWM) feedback. V_{DD1} power is supplied to an oscillating circuit that switches current into a chip-scale air core transformer. Power transferred to the secondary side is rectified and regulated to either 3.3 V or 5 V. The secondary (V_{ISO}) side controller regulates the output by creating a PWM control signal that is sent to the primary (V_{DD1}) side by a dedicated *i*Coupler data channel. The PWM modulates the oscillator circuit to control the power being sent to the secondary side. Feedback allows for significantly higher power and efficiency.

The ADuM5401/ADuM5402/ADuM5403/ADuM5404 provide a regulation control output (RC_{OUT}) signal that can be connected to other *iso*Power devices. This feature allows a single regulator to control multiple power modules without contention. When auxiliary power modules are present, the V_{ISO} pins can be connected together to work as a single supply. Because there is only one feedback control path, the supplies work together seamlessly.

The ADuM5401/ADuM5402/ADuM5403/ADuM5404 implement undervoltage lockout (UVLO) with hysteresis on the V_{DD1} power input. This feature ensures that the converter does not go into oscillation due to noisy input power or slow power-on ramp rates.

A minimum load current of 10 mA is recommended to ensure optimum load regulation. Smaller loads can generate excess noise on chip due to short or erratic PWM pulses. Excess noise generated this way can cause data corruption, in some circumstances.

PCB LAYOUT

The ADuM5401/ADuM5402/ADuM5403/ADuM5404 digital isolators with 0.5 W *iso*Power integrated dc-to-dc converters require no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins (see Figure 23). Note that a low ESR bypass capacitor is required between Pin 1 and Pin 2, as close to the chip pads as possible.

The power supply section of the ADuM5401/ADuM5402/ADuM5403/ADuM5404 uses a 180 MHz oscillator frequency to efficiently pass power through its chip-scale transformers. In addition, normal operation of the data section of the *i*Coupler introduces switching transients on the power supply pins. Bypass capacitors are required for several operating frequencies. Noise suppression requires a low inductance, high frequency capacitor; ripple suppression and proper regulation require a large value capacitor. These are most conveniently connected between Pin 1 and Pin 2 for V_{DD1} and between Pin 15 and Pin 16 for V_{ISO}.

To suppress noise and reduce ripple, a parallel combination of at least two capacitors is required. The recommended capacitor values are 0.1 µF and 10 µF for V_{DD1}. The smaller capacitor must have a low ESR; for example, use of a ceramic capacitor is advised.

Note that the total lead length between the ends of the low ESR capacitor and the input power supply pin must not exceed 2 mm. Installing the bypass capacitor with traces more than 2 mm in length may result in data corruption. A bypass capacitor between Pin 1 and Pin 8 and between Pin 9 and Pin 16 should also be considered unless both common ground pins are connected together close to the package.

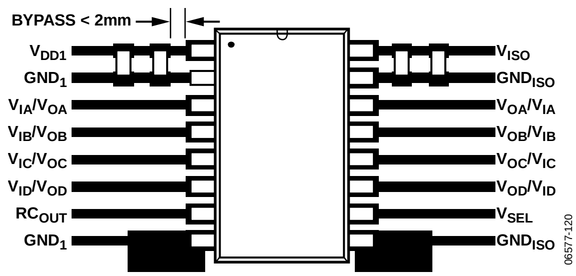


Figure 23. Recommended PCB Layout

In applications involving high common-mode transients, take care to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins, exceeding the Absolute Maximum Ratings specified in Table 8, thereby leading to latch-up and/or permanent damage.

The ADuM5401/ADuM5402/ADuM5403/ADuM5404 are power devices that dissipate about 1 W of power when fully loaded and running at maximum speed. Because it is not possible to apply a heat sink to an isolation device, the devices primarily depend on heat dissipation into the PCB through the GND pins. If the devices are used at high ambient temperatures, care should be taken to provide a thermal path from the GND pins to the PCB ground plane. The board layout in Figure 23 shows enlarged pads for Pin 8 and Pin 9. Implement large diameter vias from the pads to the ground and power planes. This reduces inductance and noise generation.

Multiple vias in the thermal pads can significantly reduce temperatures inside the chip. The dimensions of the expanded pads are left to the discretion of the designer and the available board space.

THERMAL ANALYSIS

The ADuM5401/ADuM5402/ADuM5403/ADuM5404 parts consist of four internal die attached to a split lead frame with two die attach paddles. For the purposes of thermal analysis, the die are treated as a thermal unit, with the highest junction temperature reflected in the θ_{JA} from Table 3. The value of θ_{JA} is based on measurements taken with the parts mounted on a JEDEC standard, 4-layer board with fine width traces and still air. Under normal operating conditions, the ADuM5401/ADuM5402/ADuM5403/ADuM5404 devices operate at full load across the full temperature range without derating the output current. However, following the recommendations in the PCB Layout section decreases thermal resistance to the PCB, allowing increased thermal margins in high ambient temperatures.

EMI CONSIDERATIONS

The dc-to-dc converter section of the ADuM5401/ADuM5402/ADuM5403/ADuM5404 components must operate at very high frequency to allow efficient power transfer through the small transformers. This creates high frequency currents that can propagate in circuit board ground and power planes, causing edge and dipole radiation. Grounded enclosures are recommended for applications that use these devices. If grounded enclosures are not possible, good RF design practices should be followed in the PCB layout. Refer to the AN-0971 Application Note, *Control of Radiated Emissions for isoPower Devices*, for the most current PCB layout recommendations specifically for the ADuM5401/ADuM5402/ADuM5403/ADuM5404.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component (see Figure 24). The propagation delay to a logic low output may differ from the propagation delay to a logic high.

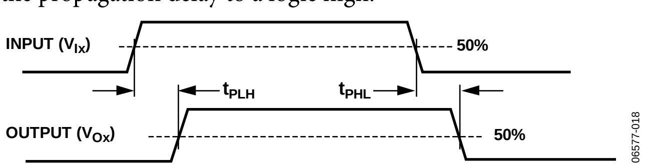


Figure 24. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the input signal timing is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM5401/ADuM5402/ADuM5403/ADuM5404 component.

Propagation delay skew refers to the maximum amount the propagation delay differs between multiple ADuM5401/ADuM5402/ADuM5403/ADuM5404 components operating under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than 1 μs, periodic sets of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses of more than approximately 5 μs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default low state by the watchdog timer circuit. This situation should occur in the ADuM5401/ADuM5402/ADuM5403/ADuM5404 only during power-up and power-down operations.

The limitation on the ADuM5401/ADuM5402/ADuM5403/ADuM5404 magnetic field immunity is set by the condition in which induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur.

The 3.3 V operating condition of the ADuM5401/ADuM5402/ADuM5403/ADuM5404 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude of >1.0 V. The decoder has a sensing threshold of about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\sum \pi r_n^2;\ n = 1, 2, \ldots, N$$

where:
β is magnetic flux density (Gauss).
r_n is the radius of the n[th] turn in the receiving coil (cm).
N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM5401/ADuM5402/ADuM5403/ADuM5404, and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 25.

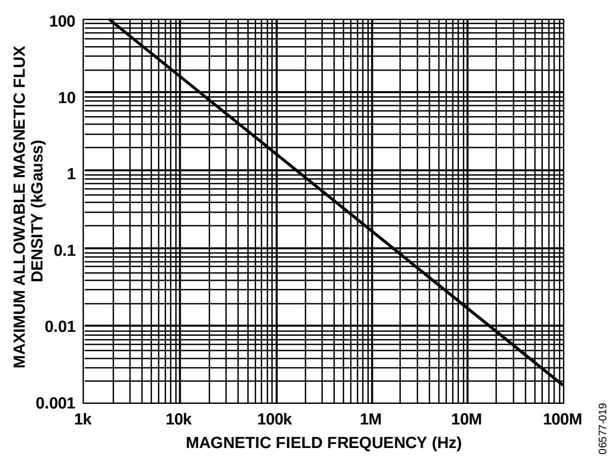


Figure 25. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kGauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V, which is still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM5401/ ADuM5402/ADuM5403/ADuM5404 transformers. Figure 26 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 26, the ADuM5401/ADuM5402/ADuM5403/ADuM5404 are immune and can be affected only by large currents operated at high frequency very close to the component. For the 1 MHz example, a 0.5 kA current would need to be placed 5 mm away from the ADuM5401/ADuM5402/ADuM5403/ADuM5404 to affect component operation.

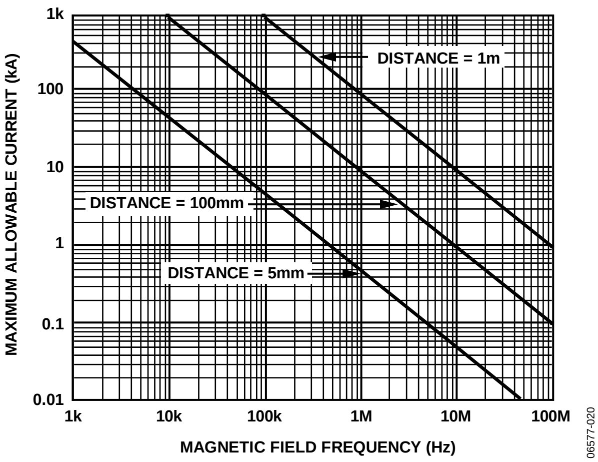


Figure 26. Maximum Allowable Current for Various Current-to-ADuM5401/ADuM5402/ADuM5403/ADuM5404 Spacings

In combinations of strong magnetic field and high frequency, any loops formed by PCB traces cand induce error voltages sufficiently large to trigger the thresholds of succeeding circuitry. To avoid this, care should be taken in the layout of such traces.

POWER CONSUMPTION

The V_{DD1} power supply input provides power to the *i*Coupler data channels, as well as to the power converter. For this reason, the quiescent currents drawn by the data converter and the primary and secondary I/O channels cannot be determined separately. All of these quiescent power demands have been combined into the $I_{DD1(Q)}$ current, as shown in Figure 27. The total I_{DD1} supply current is equal to the sum of the quiescent operating current; the dynamic current, $I_{DD1(D)}$, demanded by the I/O channels; and any external I_{ISO} load.

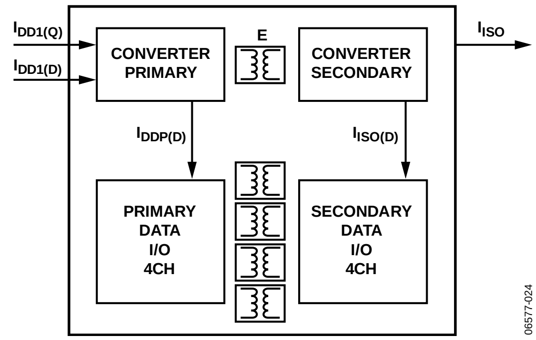


Figure 27. Power Consumption Within the ADuM5401/ADuM5402/ADuM5403/ADuM5404

Dynamic I/O current is consumed only when operating a channel at speeds higher than the refresh rate of f_r. The dynamic current of each channel is determined by its data rate. Figure 19 shows the current for a channel in the forward direction, meaning that the input is on the V_{DD1} side of the part. Figure 20 shows the current for a channel in the reverse direction, meaning that the input is on the V_{ISO} side of the part. Figure 19 and Figure 20 assume a typical 15 pF load.

The following relationship allows the total I_{DD1} current to be calculated:

$$I_{DD1} = (I_{ISO} \times V_{ISO})/(E \times V_{DD1}) + \Sigma\, I_{CHn};\ n = 1 \text{ to } 4 \quad (1)$$

where:
I_{DD1} is the total supply input current.
I_{ISO} is the current drawn by the secondary side external load.
E is the power supply efficiency at 100 mA load from Figure 11 at the V_{ISO} and V_{DD1} condition of interest.
I_{CHn} is the current drawn by a single channel determined from Figure 19 or Figure 20, depending on channel direction.

The maximum external load can be calculated by subtracting the dynamic output load from the maximum allowable load.

$$I_{ISO(LOAD)} = I_{ISO(MAX)} - \Sigma\, I_{ISO(D)n};\ n = 1 \text{ to } 4 \quad (2)$$

where:
$I_{ISO(LOAD)}$ is the current available to supply an external secondary side load.
$I_{ISO(MAX)}$ is the maximum external secondary side load current available at V_{ISO}.
$I_{ISO(D)n}$ is the dynamic load current drawn from V_{ISO} by an input or output channel, as shown in Figure 21 and Figure 22.

The preceding analysis assumes a 15 pF capacitive load on each data output. If the capacitive load is larger than 15 pF, the additional current must be included in the analysis of I_{DD1} and $I_{ISO(LOAD)}$.

POWER CONSIDERATIONS

The ADuM5401/ADuM5402/ADuM5403/ADuM5404 power input, data input channels on the primary side, and data channels on the secondary side are all protected from premature operation by UVLO circuitry. Below the minimum operating voltage, the power converter holds its oscillator inactive and all input channel drivers and refresh circuits are idle. Outputs remain in a high impedance state to prevent transmission of undefined states during power-up and power-down operations.

During application of power to V_{DD1}, the primary side circuitry is held idle until the UVLO preset voltage is reached. At that time, the data channels initialize to their default low output state until they receive data pulses from the secondary side.

When the primary side is above the UVLO threshold, the data input channels sample their inputs and begin sending encoded pulses to the inactive secondary output channels. The outputs on the primary side remain in their default low state because no data comes from the secondary side inputs until secondary power is established. The primary side oscillator also begins to operate, transferring power to the secondary power circuits. The secondary V_{ISO} voltage is below its UVLO limit at this point; the regulation control signal from the secondary is not being generated. The primary side power oscillator is allowed to free run in this circumstance, supplying the maximum amount of power to the secondary, until the secondary voltage rises to its regulation setpoint. This creates a large inrush current transient at V_{DD1}. When the regulation point is reached, the regulation control circuit produces the regulation control signal that modulates the oscillator on the primary side. The V_{DD1} current is reduced and is then proportional to the load current. The inrush current is less than the short-circuit current shown in Figure 14. The duration of the inrush depends on the V_{ISO} loading conditions and the current available at the V_{DD1} pin.

As the secondary side converter begins to accept power from the primary, the V_{ISO} voltage starts to rise. When the secondary side UVLO is reached, the secondary side outputs are initialized to their default low state until data is received from the corresponding primary side input. It can take up to 1 μs after the secondary side is initialized for the state of the output to correlate with the primary side input.

Secondary side inputs sample their state and transmit it to the primary side. Outputs are valid about 1 μs after the secondary side becomes active.

Because the rate of charge of the secondary side power supply is dependent on loading conditions, the input voltage, and the output voltage level selected, take care with the design to allow the converter sufficient time to stabilize before valid data is required.

When power is removed from V_{DD1}, the primary side converter and coupler shut down when the UVLO level is reached. The secondary side stops receiving power and starts to discharge. The outputs on the secondary side hold the last state that they received from the primary side. Either the UVLO level is reached and the outputs are placed in their high impedance state, or the outputs detect a lack of activity from the primary side inputs and the outputs are set to their default low value before the secondary power reaches UVLO.

INCREASING AVAILABLE POWER

The ADuM5401/ADuM5402/ADuM5403/ADuM5404 are designed with the capability of running in combination with other compatible *iso*Power devices. The RC_{OUT} pin allows the ADuM5401/ADuM5402/ADuM5403/ADuM5404 to provide its PWM signal to another device acting as a master to regulate its self and slave devices. Power outputs are combined in parallel while sharing output power equally.

The ADuM5401/ADuM5402/ADuM5403/ADuM5404 can only be a master/standalone, and the ADuM5200 can only be a slave/standalone device. The ADuM5000 can operate as either a master or slave. This means that the ADuM5000, ADuM520x, and ADuM540x can only be used in the master slave combinations listed in Table 15.

Table 15. Allowed Combinations of *iso*Power Parts

	Slave		
Master	**ADuM5000**	**ADuM520x**	**ADuM540x**
ADuM5000	Yes	Yes	No
ADuM520x	No	No	No
ADuM540x	Yes	Yes	No

The allowed combinations of master and slave configured parts listed in Table 15 is sufficient to make any combination of power and channel count.

Table 16 illustrates how *iso*Power devices can provide many combinations of data channel count and multiples of the single unit power.

Table 16. Configurations for Power and Data Channels

	Number of Data Channels			
Power Units	**0**	**2**	**4**	**6**
1-Unit Power	ADuM5000 master	ADuM520x master	ADuM5401 to ADuM5404 master	ADuM5401 to ADuM5404 master ADuM121x
2-Unit Power	ADuM5000 master ADuM5000 slave	ADuM5000 master ADuM520x slave	ADuM5401 to ADuM5404 master ADuM520x slave	ADuM5401 to ADuM5404 master ADuM520x slave
3-Unit Power	ADuM5000 master ADuM5000 slave ADuM5000 slave	ADuM5000 master ADuM5000 slave ADuM520x slave	ADuM5401 to ADuM5404 master ADuM5000 slave ADuM5000 slave	ADuM5401 to ADuM5404 master ADuM520x slave ADuM5000 slave

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. Analog Devices conducts an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM5401/ADuM5402/ADuM5403/ADuM5404.

Accelerated life testing is performed using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined, allowing calculation of the time to failure at the working voltage of interest. The values shown in Table 9 summarize the peak voltages for 50 years of service life in several operating conditions. In many cases, the working voltage approved by agency testing is higher than the 50-year service life voltage. Operation at working voltages higher than the service life voltage listed leads to premature insulation failure.

The insulation lifetime of the ADuM5401/ADuM5402/ADuM5403/ADuM5404 depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates, depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 28, Figure 29, and Figure 30 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. A 50-year operating lifetime under the bipolar ac condition determines the Analog Devices recommended maximum working voltage.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 9 can be applied while maintaining the 50-year minimum lifetime, provided the voltage conforms to either the unipolar ac or dc voltage cases. Any cross-insulation voltage waveform that does not conform to Figure 29 or Figure 30 should be treated as a bipolar ac waveform, and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 9.

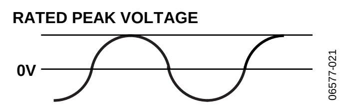


Figure 28. Bipolar AC Waveform

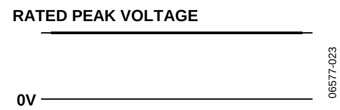


Figure 29. DC Waveform

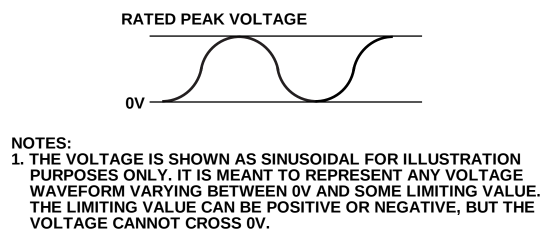


Figure 30. Unipolar AC Waveform

OUTLINE DIMENSIONS

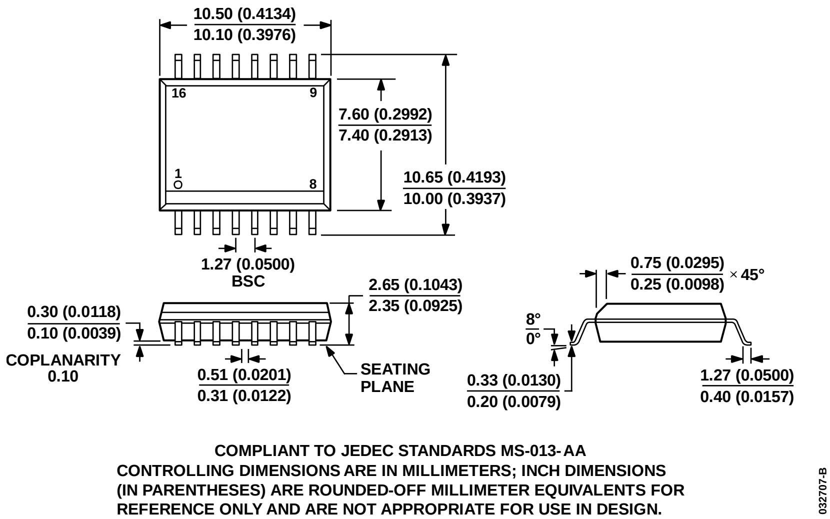


Figure 31. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{ISO} Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Pulse Width Distortion (ns)	Temperature Range (°C)	Package Description	Package Option
ADuM5401ARWZ[1, 2]	3	1	1	100	40	−40 to +105	16-Lead SOIC_W	RW-16
ADuM5401CRWZ[1, 2]	3	1	25	60	6	−40 to +105	16-Lead SOIC_W	RW-16
ADuM5402ARWZ[1, 2]	2	2	1	100	40	−40 to +105	16-Lead SOIC_W	RW-16
ADuM5402CRWZ[1, 2]	2	2	25	60	6	−40 to +105	16-Lead SOIC_W	RW-16
ADuM5403ARWZ[1, 2]	1	3	1	100	40	−40 to +105	16-Lead SOIC_W	RW-16
ADuM5403CRWZ[1, 2]	1	3	25	60	6	−40 to +105	16-Lead SOIC_W	RW-16
ADuM5404ARWZ[1, 2]	0	4	1	100	40	−40 to +105	16-Lead SOIC_W	RW-16
ADuM5404CRWZ[1, 2]	0	4	25	60	6	−40 to +105	16-Lead SOIC_W	RW-16

[1] Tape and reel are available. The addition of an RL suffix designates a 13” (1,000 units) tape and reel option.
[2] Z = RoHS Compliant Part.

NOTES

NOTES